First Semester M.Tech. Degree Examination, Dec.2014/Jan.2015
Digital System Design using Verilog

Time: 3 hrs.   Max. Marks:100

Note: *Answer any FIVE full questions.*

1 a. Assuming two vats in factory, write the verilog code for a vat buzzer to maintain the temperature between 25°C and 30°C. The buzzer should be activated if temperature is too high or too low or the vat level is too low. A switch is provided help in selecting any one vat at any time. Draw the buzzer circuit.   **(10 Marks)**

   b. With neat flowchart, describe the design methodology for hardware/software codesign.
                                                                     (07 Marks)

   c. Define the terms setup time, hold time of flip-flop.   **(03 Marks)**

2 a. Write a verilog code for 10:1 multiplexer using case statement.   **(10 Marks)**

   b. Design a priority encoder for use in domestic burglar alarm that has sensors for each zone. Each sensor signal is one when an intrusion is detected in that zone, and zero otherwise. The encoder has three bits output with zone 1 having highest priority, down to zone 8 having lowest priority. Develop the verilog code for the same.   **(10 Marks)**

3 a. With necessary equations show two alternate implementations of fast-carry-chain full adder cells used in an adder.   **(10 Marks)**

   b. With a neat figure, explain the equality comparator and in-equality comparator.   **(10 Marks)**

4 a. Develop a datapath to perform a complex multiplication of two complex numbers. The operands and products are all in Cartesian form. The real and imaginary are all in Cartesian form. The real and imaginary parts of operands are represented as signed fixed point numbers with 4 pre-binary-point and 12 post-binary-point bits. The real and imaginary parts of product are similarly represented, but with 8 pre-binary-point and 24 post-binary-point bits. Also develop verilog model of the same.   **(12 Marks)**

   b. Design a circuit that counts 16 clock cycles and produces a control signal CHr that is '1' during every tenth and twelfth cycle.   **(08 Marks)**

5 a. Design a 1G × 8-bit composite memory using 256M × 8 – bit components.   **(08 Marks)**

   b. Develop a verilog model of a dual-port 4K × 16bit flow-through SSRAM. One port allows data to be written and read, while the other port only allows data to be read.   **(08 Marks)**

   c. Determine whether there is an error in the ECC word 110111000110, and if so, correct it.
                                                                     (04 Marks)

6 a. Explain the internal organization of CPLD, with neat diagram.   **(08 Marks)**

   b. Mention the different types of Gumnut instructions set. Describe any five.   **(12 Marks)**

7 a. Design an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in system. Also develop verilog model for designed input controller.   **(12 Marks)**

   b. Discuss the following serial interface standards for connecting I/O devices:
      i) RS – 232   ii) Fire-wire.   **(08 Marks)**

8 a. What are advantages of BIST techniques? Explain 4-bit LFSR, with block diagram.
                                                                     (10 Marks)

   b. Briefly explain the design optimization.   **(10 Marks)**

* * * * *